Tools

Rapid Prototyping of Application-Specific Signal Processors

Vista Technologies, Inc.

Vista develops innovative design entry tools for hardware description language (HDL)-based designs. Vista’s StateVision and DesignVision tools graphically specify a wide range of behavior. Vista recently released the Object-Oriented VHDL (OO-VHDL) pre-processor. Vista is further developing its entry point tools to generate models and test benches in OO-VHDL.

Focus on RASSP

Object-oriented VHDL modeling is a new, RASSP-generated technology driver that will provide the modeling and reuse capability required to achieve 4X design productivity gains in the RASSP design environment.

Abstract models use high-level data types and represent the overall function of the system. They are developed early in the design process by ignoring lower-level detail that may not be understood when the models are generated.

OO-VHDL is an excellent language for specifying abstract models of architecture design using methodologies being implemented in RASSP. For example, iterative refinement of the design is well supported by OO-VHDL (object) models because they span several levels of abstraction, and they can help transition to component models that represent actual hardware.

In a RASSP design that involves multiple subsystems, boards, and modules, abstract models at the system- and architecture-level help users verify requirements and evaluate design alternatives through performance and other measurements. VHDL models of lower-level components can be used for functional and timing verification of the design.
Vista’s OO-VHDL language extension promotes model reuse through inheritance among component classes. Vista’s goal is to bring the benefits of OO-VHDL quickly and inexpensively to RASSP users by making the extension language simulatable with current simulators.

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Vista’s recently released pre-processor translates OO-VHDL constructs into standard VHDL.

The pre-processor uses an object library with reusable, generic class objects and design-specific class hierarchies. The complete OO-VHDL simulation environment will consist of the OO-VHDL pre-processor; a traceability tool that interactively maps constructs in OO-VHDL into VHDL, and vice versa, for easy debugging; and textual and graphical design entry/modeling tools.

Vista’s design entry tools, DesignVision and StateVision, provide graphical representation of behavior for modeling, viewing simulation results, and documentation. They are ideal platforms to build enhancements and new capabilities to support RASSP modeling activities.

DesignVision graphically represents a behavioral model as a collection of concurrent threads. Each thread represents a series of events and actions. As each event occurs during simulation, the corresponding action is performed.

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The StateVision tool provides a graphical front-end for specifying hierarchical state machines, produces synthesizable VHDL code, and it can describe a wide variety of state machine models. Both tools integrate with popular commercial VHDL simulators to provide graphical debugging and cross probing. Enhancements to these tools will provide the abstract modeling and simulation capabilities needed for architectural-level design in RASSP.

For More Information
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